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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,395	12/30/2003	Vasudevan Srinivasan	42P18068	8966

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EXAMINER	
KENDALL, CHUCK O	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,395	SRINIVASAN ET AL.	
	Examiner	Art Unit	
	Chuck O. Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 7/6/04, 8/29/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This is in response to the application filed on 12/30/03.

2. Claims 1 – 27 have been examined.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18 – 20 are rejected under 35 U.S.C. 101 because, claims recites a machine accessible medium which is defined in the specification in paragraph [0051] to include carrier waves and signals. And based on the Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility:

> " Claims that recite nothing but the physical characteristics of a form of energy, such as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory natural phenomena. O'Reilly, 56 U.S. (15 How.) at 112-14. Moreover, it does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in Sec. 101."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1,2, 7 – 9, 21, 22, and 25 – 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Asai et al. US 5,903,730.

Regarding claims 1,18 and 21, Asai anticipates a method, and machine accessible medium and system comprising:

determining processor utilization in a data processing system (FIG. 11, and all associated text); and

synchronizing execution of a plurality of threads in the data processing system to prevent interrupting the determining of the processor utilization (4:45 – 50).

Regarding claims 2,19 and 22, the method of claim 1, further including processing the plurality of threads simultaneously on a plurality of logical processors (4:45 – 50, see parallel processing).

Regarding claim 6 and 25, the method of claim 1, further including processing the plurality of threads simultaneously on a plurality of physical processors (FIG.11, see S18a and all associated text).

Regarding claims 7 and 26, the method of claim 6, wherein the determining includes one of the plurality of physical processors determining the processor utilization (FIG. 11, s18a – i, and all associated text).

Regarding claims 8 and 27, the method of claim 7, wherein synchronizing the execution of the plurality of threads comprises executing a predetermined unit of code on the plurality of physical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization (FIG. 8, see S15a and S15e).

Regarding claim 9, the method of claim 8, wherein determining the processor utilization comprises calculating a frequency of the one of the plurality of physical processors (FIG. 15e, see calculating the execution time of each parallel).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 3 – 5, and 10 – 17, 20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. US 5,903,730 in view of Tovinkere US 2004/0199919 A1.

Regarding claims 3 and 23, Asai discloses all the claimed limitations as applied in claim 2 above as well as the determining including one of the plurality of processors determining the processor utilization (4:7 – 15, see analyzing contents and profile information, also see FIG. 11 and all associated text). Asai doesn't expressly disclose whether they are logical processor. However Tovinkere in an analogous art and similar configuration discloses performance of logical processors (0043). Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Tovinkere, because it would enable determining processor utilization for a logical processor.

Regarding claims 4 and 24, the method of claim 3, wherein the synchronizing further includes executing a predetermined unit of code on the plurality of logical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization (Asai, FIG. 8, see S15a and S15e).

Regarding claims 5 and 20, the method of claim 4, wherein determining the processor utilization comprises calculating a frequency of the one of the plurality of logical processors (Asai, FIG. 15e, see calculating the execution time of each parallel).

Regarding claim 10, Asai discloses method comprising: determining processor utilization in a system executing at least a first thread and a second thread (Asai, 2:7 – 10, shows a plurality of routines, each thread here would equivalent to a routine).

Asai doesn't expressly disclose pausing execution of the second thread during the determining of the processor utilization. However, Tovinkere in an analogous art and similar configuration discloses that each logical processor can be individually halted to execute a specified processor thread independent of other logical processor (0002).

Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Tovinkere, because it would enable determining processor utilization of specified processes.

Regarding claim 11, the method of claim 10, further comprising executing at least the first and the second threads simultaneously on at least a first processor and a second processor in the system (Asai, 4:45 – 50, see parallel processing).

Regarding claim 12, the method of claim 10, the determining including the first processor determining the processor utilization (Asai, 4:7 – 15, see analyzing contents and profile information, also see FIG. 11 and all associated text).

Regarding claim 13, Asai discloses an apparatus comprising:

a plurality of processors, one of the plurality of processors to determine processor utilization and the remaining processors to execute a predetermined unit of code to prevent interrupting the one determining the processor utilization (FIG. 11, and all associated text). Asai doesn't expressly disclose a bus coupling the plurality of processors to each other. However, Tovinkere in an analogous art and similar configuration discloses two or more processors electrically coupled by a system to one or more primary devices (0015). Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Tovinkere, because it would enable interconnectivity between the processors.

Regarding claim 14, the apparatus of 13, further comprising a performance monitor counter coupled to each of the plurality of processors to keep track of when the processor is active (Asai, FIG. 11).

Regarding claim 15, the apparatus of 14, the performance monitor counter to provide a count for determining the processor utilization (Asai, 8:32 – 36).

Regarding claim 16, the apparatus of claim 13, wherein the plurality of processors comprise a plurality of logical processors to execute threads simultaneously (Asai, FIG.1, 12a – 12c, also see Tovinkere FIG.2, 104).

Regarding claim 17, Asai discloses all the claimed limitations as applied in claim 13 above. Asai doesn't expressly disclose pausing the remaining processors. However, Tovinkere in an analogous art and similar configuration discloses that each logical processor can be individually halted to execute a specified processor thread independent of other logical processor (0002). Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Tovinkere, because it would enable determining processor utilization of specified processes.

Correspondence information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.

ck 2/5/07